24V 4A Sourcing Current and Sinking Current Single-channel Driver

1. Features

- 5-pin SOT-23 package;
- 4A peak sourcing current and sinking current
- Wide-range VDD power supply as high as 24V
- VDD under-voltage protection, 4.5V to 20V recommended working voltage
- Dual-input design with both configuration of positive input and that of inverted input. The not used input pin can be used for enabling or disenabling control.
- Negative voltage input as low as -5V
- Compatible to TTL and CMOS input level
- Low propagation delay (with the typical value lower than 20ns)
- Output low level during input floating
- Working temperature ranges of -40℃ to 125℃

2. Applications

- Switching power supply
- Motor control
- AC/DC and DC/DC converter
- Server and rectifier for communication equipment
- EV/HEV inverter and DC/DC convertor
- PV voltage rise and inverter
- UPS
- Applied to emerging broad-band gap power element driver

3.Description

The SL27517 is a single-channel 4A high-speed low-side gate driver that efficiently and safely drives MOSFETs, IGBTs, and emerging wide-bandgap power devices. With characteristics of low propagation delay and compact SOT-23, it can achieve the MOSFET switching frequency of hundreds of kHz. The chip is applicable to synchronous rectification driving of servers and communication power supply. In this condition, the dead time of the synchronous tube MOSFET leads to direct influence on efficiency of the converter.

The 4.5V to 20V wide ranges VDD supply voltage can drive MOSFET or GaN power devices effectively. The integrated UVLO protective function can ensure the output low level in abnormal conditions.

The -5V to 24V independent input pin voltage ranges can ensure stable working in condition of over-shoot caused by stray inductance. The voltage threshold value of the input pin is compatible to the TTL level input.
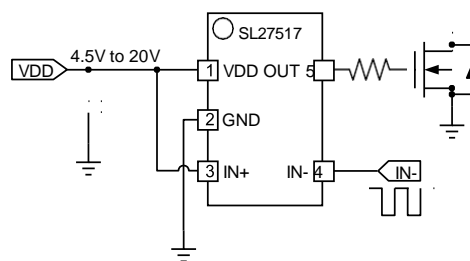
Information of the device

Information of the device	Package	Package
SL27517	SOT-23-5	Tape and Reel

Typical application drawing
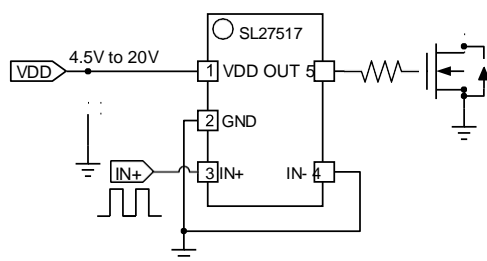
Positive-going input

Inverted input

Contents

4.Configuration and functions of pins

Top view of SOT-23-5

```
            SL27517
VDD  [1]              [5]  OUT

GND  [2]

IN+  [3]              [4]  IN-
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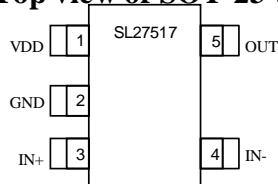
Functions of pins

pin	Name	I/O	Description
1	VDD	P	Supply voltage
2	GND	G	Ground
3	IN+	I	Positive-going input
4	IN-	I	Inverted input
5	OUT	O	Output

Truth-value table

The voltage of VDD is higher than the threshold voltage of UVLO

IN+	IN-	OUT
Low or suspended	Any level	Low
Any level	High or suspended	Low
Height	Low	Height

5. Technical indexes

5.1 Absolute Max. rated value

Within the ranges of indoor temperature (unless otherwise specified) [1]

		MIN	MAX	Unit
V_{DD}	Supply voltage (relative to ground)	-0.3	24	V
OUT	grid driving output voltage	-0.3	V_{DD}+0.3	V
IN+, IN-	signal input voltage	-5.0	24	V
T_J	Junction temperature	-40	150	℃
T_{STG}	storage temperature	-65	150	℃

[1] If the operation exceeds the ranges listed in the "absolute maximum rated value", it may lead to permanent damages to the device. Long-term exposure to the absolute maximum rated value conditions may lead to influences on reliability of the device. Long-time working at can the absolute rated conditions may lead to influences on reliability of the chip.

5.2 Anti-static level

		Value	Unit
$V_{(ESD)}$	Human body model(HBM)，ANSI/ESDA/JEDEC JS-001 [1]	+/-2000	V
	Charged device model (CDM)，JEDEC specification JESD22-C101 [2]	+/-500	

(1) As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 500V HBM. As specified in JEDEC document JEP155, the standard ESD control process is allowed for safe manufacturing for 250V CDM.

5.3 Recommended working conditions

		MIN	MAX	Unit
V_{DD}	Supply voltage	4.5	20	V
IN+, IN-	signal input voltage	0	20	V
T_A	environment temperature	-40	125	℃

5.4 Thermal resistance information

	Value	Unit
RθJA junction temperature – environment thermal resistance	165	℃/W
RθJB junction temperature – PCB thermal resistance	55	℃/W

5.5 Electrical specifications

Unless otherwise specified, V_{DD} = 12 V, TA = –40°C to 125°C

In the environment of 25°C, in the designated pin, the positive-going current is input, and the inversed current is output.

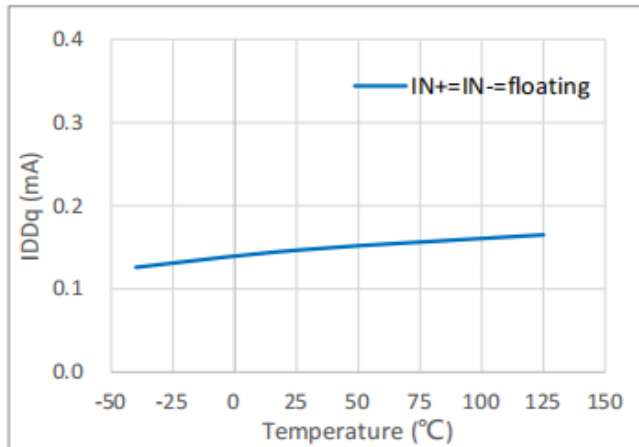| Parameters	Testing conditions	MIN	Typical	MAX	Unit
Bias current					
I_{DDoff} Starting current	V_{DD}=3V, IN=0V		67		µA
I_{DDq} Quiescent current	IN=0V		150		µA
Undervoltage protection					
V_{ON} under voltage threshold value	Rise threshold value		3.8	4.2	V
V_{OFF}	Drop threshold value	3.2	3.5		
input (IN+, IN-)					
V_{INH} input rise threshold value			2.0	2.4	V
V_{INL} input drop threshold value		0.8	1.2		V
V_{INHYS} input hysteresis			0.8		V
V_{INHYS} Negative voltage input		-5			V
Output					
I_O Sourcing and sinking current peak	C_{LOAD} =0.22uF, With external current limiting resistor, 1kHz switching frequency		4.0		A
V_{OH} output high level	I_{OUTH} = -10mA		V_{DD}-0.056	V_{DD}-0.12	V
V_{OL} output low voltage	I_{OUTL} = 10mA		0.0054	0.012	V
R_{OH} output quiescent pull-up resistance			5.6	12	Ω
R_{OL} output pull-down resistance			0.54	1.2	Ω
Time series					
TD_{ff} rise delay TD_{rr} drop delay	Cload = 1.8nF		16 16	30 30	ns
T_f rise time T_r drop time	Cload = 1.8nF		6 6		ns

6. Typical Characteristics

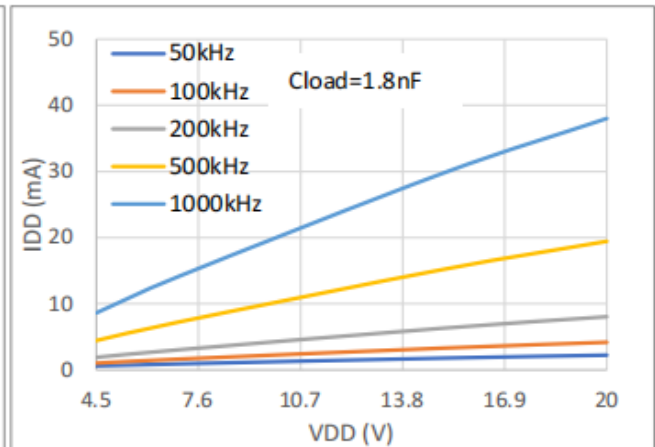**Figure 1. Quiescent current IDDq vs temperature**
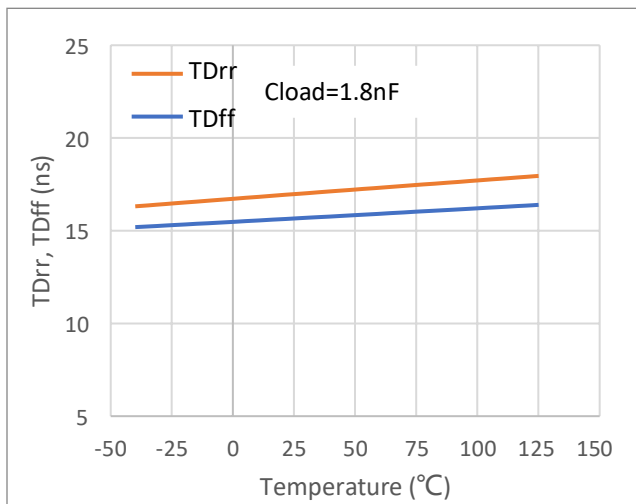

Figure 2. Working current IDD vs VDD

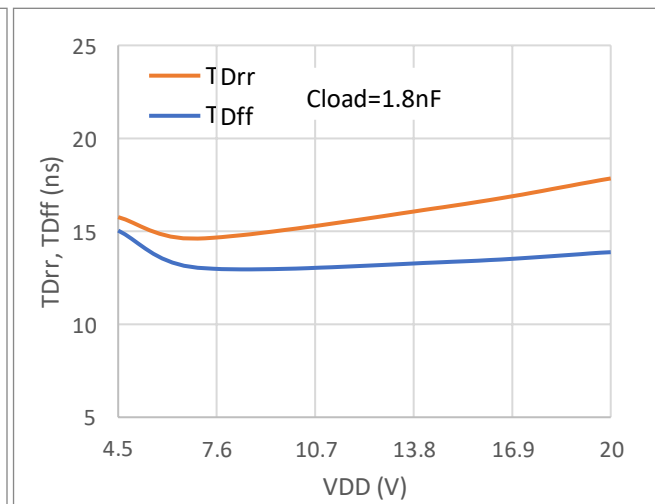**Figure 3. Propagation delay vs temperature**
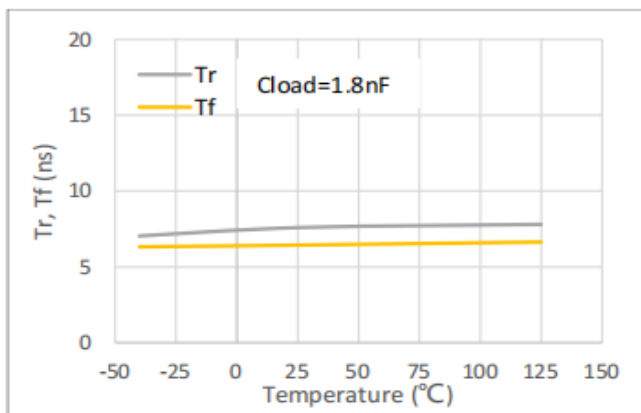

Figure 4. Propagation delay vs VDD
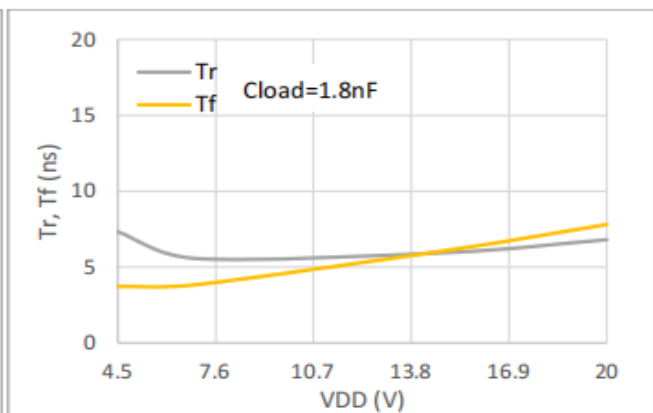

Figure 5. Rise time and drop time vs temperature


Figure 6. Rise time and drop time vs VDD

7. Detailed description

The SL27517 driver provides single-channel high-speed low-side gate drive.

7.1 Signal Input

IN+ is the positive logic gird driving input, and IN- is the reverse logic grid driving input. The two pins are the weak pull-down input and the week pull-up input, respectively, If the input is kept floating, the output will be pulled to the ground. The input is the TTL and CMOS compatible logic level, with the maximum input tolerance of 20V.

Functional block diagram
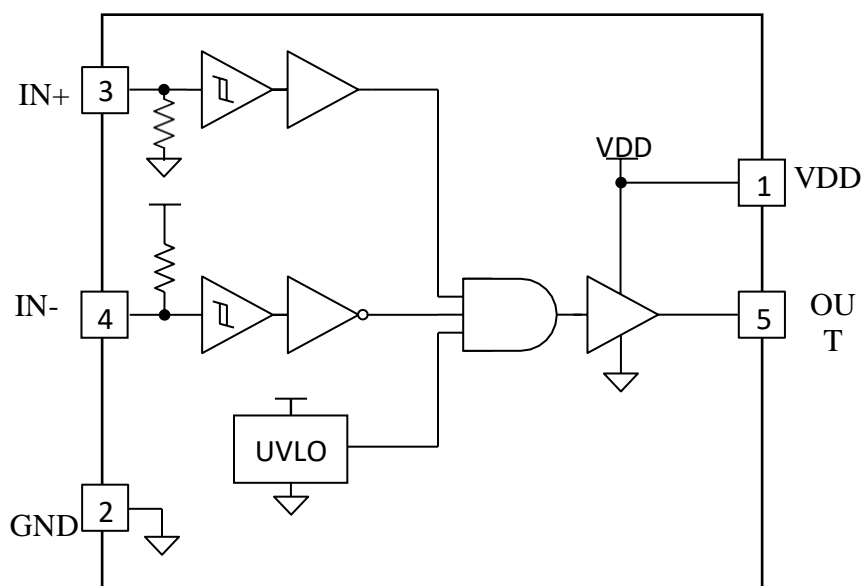
7.2 OUT

OUT consists of a pair of composite pull-up P-type plus N-type MOSFETs and a pull-down N-type MOSFET. The output of the SL27517 can provide 4A peak source and sink current pulses. The output voltage swings rail-to-rail between VDD and GND. The body diode of the MOSFET also provides a voltage clamping path to limit the output voltage above or below this range. In many cases, external Schottky diode clamping is not necessary.

7.3 VDD and undervoltage protection

The maximum rated input voltage of the SL27517 is 24V. The SL27517 can meet the gate drive requirements of Si MOSFETs, IGBTs, and SiC MOSFETs. The driver has an under-voltage protection function inside. When VDD is below the under-voltage protection threshold, the driver will ignore the input signal and drive the output low.
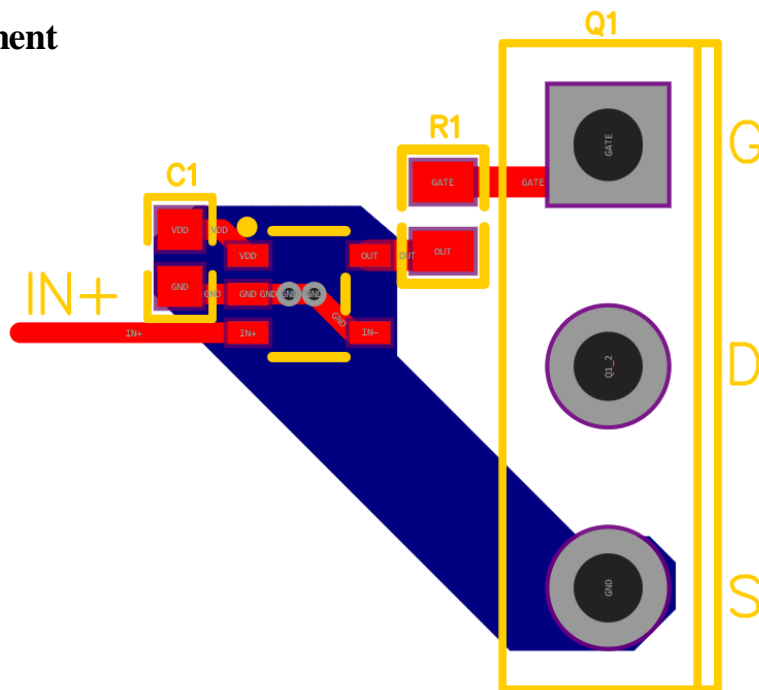
8. Application and realization
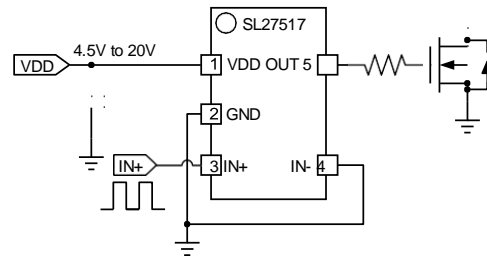
Positive-going input
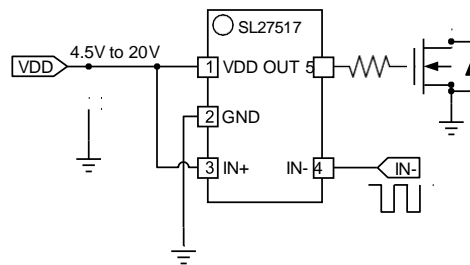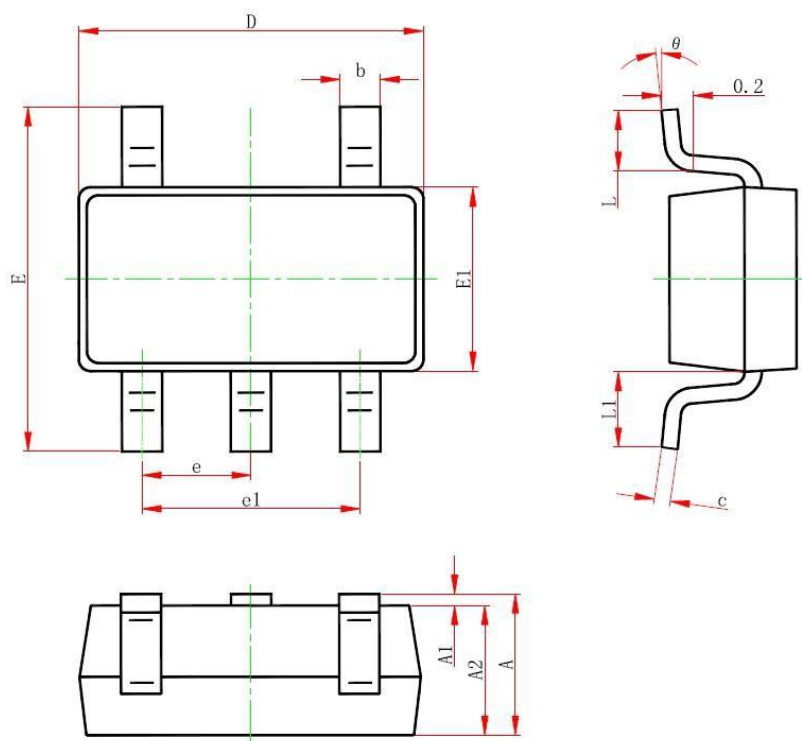

Reverse input

9. PCB arrangement

SL27517Arrangement example

10. Package information

SOT-23-5 package dimension

Symbol	Dimension (mm)		Dimension (inch)	
	Min	**Max**	**Min**	**Max**
A	0.900	1.450	0.035	0.057
A1	0.000	0.150	0.000	0.006
A2	1.100		0.043	
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.750	3.050	0.108	0.120
E1	1.450	1.750	0.057	0.069
E	2.600	3.000	0.102	0.118
e	0.950		0.037	
e1	1.900		0.075	
L	0.300	0.600	0.012	0.024
L1	0.600		0.024	
θ	0.000	8.000	0.000	0.315